AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0003] as follows:

[0003] FIG. 1 is a block diagram of a general Moving Picture Experts Group – 2 (MPEG-2) video decoding system. Referring to FIG. 1, the MPEG system decoding system includes an MPEG system decoder 101, a video decoder 102, a video display processor (VDP) 103, an audio decoder 104, a memory interface 105, and a host interface 106. Further, an external DRAM memory is connected to the memory interface 105. The external DRAM memory stores input bitstreams and frame-buffers for motion compensation. In order to support an MP@HL mode in ~~MPGE-2~~MPEG-2 standard as shown in FIG. 1, bit-buffer size of about 10 Mbits is required and a maximum allowable bit rate reaches about 80 Mbit/s.

Please amend paragraph [0050] as follows:

[0050] FIG. 5 shows a frame structure of the DV 525-60 system. Referring to FIG. 5, in the case of the DV format, the signal is transmitted by supper block unit consisting of 27 adjacent macro blocks. The transmitted supper block is positioned randomly in a regular pattern within an external frame memory. In other words, the macro blocks transmitted like MPEG video are not positioned sequentially by slice unit and transmitted without being adjacent like the ~~supper~~ super block. Therefore, the de-shuffler 309 is needed for the reconfiguration of the original screen.